IEEE Albuquerque SSCS/EDS Chapter Inaugural Talk :

PART I: ***The Road to Gate-All-Around CMOS*** *(07/17 -- 12:10PM)*

Despite the much debated end of Moore's Law, CMOS scaling still maintains economic relevance with 2nm gate-all-around SoCs anticipated in the coming quarters. Area scaling extensively driven by design/technology innovations co-optimized for primarily logic scaling continue to offer compelling node-to-node power, performance, area, and cost benefits. In this tutorial, we will start with a walk through memory lane, recounting a brief history of transistor evolution to motivate the migration from the planar MOSFET to the fully depleted FinFET. We will summarize the key process technology elements that have enabled the finFET CMOS nodes, highlighting the resulting technology characteristics and challenges. This will set the stage for transitioning to the nanoribbon gate-all-around (GAA) transistor architecture and unveiling the magic of how these devices are fabricated.

PART II: ***The Road to Gate-All-Around and Its Impact on Analog Design*** *(07/17 -- 2:30PM)*

Embrace the technology – the essence of how analog design has adapted and thrived throughout decades of increasingly unfriendly CMOS scaling. This presentation will cover the impact of advanced CMOS on analog design, and examples of the creativity of analog designers to preserve and extend the performance of traditional analog functions. We will finally take a look at technologies on the horizon and suggest how they will impact the future of analog design based on the challenges that CMOS scaling has imposed. To address the growing effort required for analog/mixed-signal design, we will cover design strategies on how analog design has adapted and thrived through decades of increasingly unfriendly scaling, including the migration to ***heterogeneous integration***.

Hosted by: Intel NMDM TLD

Dr. Alvin Loke

Presented by: ***Dr. Alvin Loke***

Dr. Alvin Loke is a Senior Principal Engineer at Intel, San Diego, working on analog design/technology co-optimization for Intel's gate-all-around (GAA) CMOS. He has previously worked on CMOS nodes spanning 250nm to 2nm at Agilent, AMD, Qualcomm, TSMC, and NXP. Alvin received a MS and PhD from Stanford. After several years in CMOS process integration, he has since worked on analog/mixed-signal design focusing on a variety of wireline links including chiplet IOs, design/model/technology interface, and analog design methodologies. Alvin currently serves as the VLSI Symposium Secretary, IEEE Solid-State Circuits Society (SSCS) Global Chapters Chair, and as a SSCS Distinguished Lecturer. Alvin frequently speaks on CMOS technology and its impact on analog design, having authored invited publications including the CICC 2018 Best Paper and short courses at ISSCC, VLSI Symposium, CICC, and BCICTS.

Join us on 07/17th starting at 12:10PM MST. In person or online via TEAMS.
Address: 1600 Rio Rancho Blvd SE, Rio Rancho, NM 87124. Building: RR5. Room: RR5-1NEO.

TEAMS: https://teams.microsoft.com/meet/263943600883264?p=NzgmHR9oWlj2XY1HA9